IN THE SPECIFICATION:

Please replace paragraph number **[0007]** with the following rewritten paragraph:

[0007] As shown in FIG. 1D, an electrically conductive material 22, *e.g.*, tungsten, is subsequently blanket deposited over the interlevel dielectric layer 14 such that the trace depressions 18 are filled therewith. The electrically conductive material 22 is then planarized using, *e.g.*, a mechanical abrasion technique, such as chemical mechanical planarization (CMP), to isolate the electrically conductive material 22 in the trace depressions 18, as illustrated in FIG. 1E. Thus, a semiconductor device structure 24 including a plurality of traces 26 in the interlevel dielectric layer 14 thereof is fabricated.

Please replace paragraph number **[0018]** with the following rewritten paragraph:

[0018] The present invention, in one embodiment, includes a method for creating depressions in a semiconductor substrate using laser machining processes and using such depressions to define precise electrical pathways in a semiconductor device structure. The method includes providing a semiconductor substrate (*e.g.*, a silicon wafer) and forming one or more electrical pathways in the semiconductor substrate using laser machining processes. The electrical pathways may subsequently be filled with an electrically conductive material (*e.g.*, a metal, a conductive polymer, or conductive nano-particles) and planarized to create one or more elongated conductive elements in the semiconductor substrate. It will be understood by those of ordinary skill in the art that if the semiconductor substrate is formed of a conductive semiconductor material such as silicon (*e.g.*, a silicon substrate used for test purposes), an insulating layer comprising an insulating material, such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or parylene, may be deposited or grown on the surface of the semiconductor substrate prior to ~~filing~~ filling the electrical pathways therein with the electrically conductive material.

Please replace paragraph number **[0027]** with the following rewritten paragraph:

[0027] FIG. 3F is a top plan view of a semiconductor device having a plurality of filled elongated conductive elements in a semiconductor substrate ~~thereof~~ thereof;

Please replace paragraph number **[0030]** with the following rewritten paragraph:

[0030] FIGs. 5A-5E are side cross-sectional views schematically illustrating a method (in accordance with the present invention) for forming elongated conductive elements (*e.g.*, traces) ~~in~~ in a semiconductor substrate concurrently with the formation of a discrete conductive structure, *e.g.*, a conductive via;

Please replace paragraph number **[0034]** with the following rewritten paragraph:

[0034] FIG. 7 is a side view ~~of~~ of a semiconductor device, *e.g.*, a cellular telephone/Personal Digital Assistant (PDA) combination unit, which includes a plurality of stacked chips, such device having precise vertical electrical connections formed through the thickness of multiple chips in the stack; and

Please replace paragraph number **[0041]** with the following rewritten paragraph:

[0041] Referring now to FIG. 3B, a desired pattern of one or more trace precursors in the form of trace depressions 108 may be formed in a surface 103 of the semiconductor substrate 104 using a focused laser beam 110. In practice, one would place a semiconductor wafer, or other suitable semiconductor substrate 104, on a platen of a suitable laser machining apparatus. The desired pattern of trace depressions 108 may be stored in a software program associated with the laser machining apparatus such that upon activation of the laser machining apparatus, the desired pattern may be ablated in the surface of the semiconductor substrate 104. In doing so, the focused laser beam 110 rapidly traverses the ~~surface~~ surface 103 of the semiconductor substrate 104, pausing briefly in those locations where a trace depression 108 is desired. Due to the rapidity of the process, the method of the present invention would typically be carried out at the wafer level.

Please replace paragraph number **[0042]** with the following rewritten paragraph:

[0042] Currently available lasers in semiconductor device manufacturing plants have a minimum focused laser beam 110 width or footprint of approximately 15 microns, or smaller. Accordingly, the technology of the present invention enables the formation of trace depressions 108 having a width as small as approximately 15 microns, or smaller, and a shape suitable to define the desired trace pattern. A suitable laser machining apparatus for forming the trace depressions 108 is Model No. 2700 manufactured by Electro Scientific, Inc., of Portland, OR. Another suitable laser machining apparatus is manufactured by General Scanning of ~~Sommerville,~~ Somerville, Mass. and is designated as Model No. 670-W. Yet another suitable laser machining apparatus for forming the trace depressions 108 is manufactured by Synova S.A., Lausanne, Switzerland.

Please replace paragraph number **[0043]** with the following rewritten paragraph:

[0043] A representative laser fluence for forming the trace depressions 108 through a semiconductor substrate 104 (*e.g.*, a silicon wafer) having a thickness of about 28 mils (725 μm), is from about 2 to about 10 watts/~~per~~ opening at a pulse duration of 20-25 NS, and at a repetition rate of up to several thousand per second. The wavelength of the focused laser beam 110 may be a standard UV wavelength (*e.g.*, 355 nm) or green wavelength (*e.g.*, 1064 nm-532 nm). By way of example, the width of the trace depressions 108 can be from about 10 μm to about 2 mils or greater.

Please replace paragraph number **[0044]** with the following rewritten paragraph:

[0044] It will be understood and appreciated by those of ordinary skill in the art that the footprint of the focused laser beam 110 is limited only by the available optics. Thus, as optical technology advances, the footprint of the focused laser beam 110 will become reduced in dimension, such that trace depressions 108 having increasingly smaller widths may be formed utilizing the technology of the present invention.

Please replace paragraph number **[0047]** with the following rewritten paragraph:

[0047] An electrically conductive material 112 may subsequently be blanket coated over the etched semiconductor substrate 104 using a suitable deposition process such that the trace depressions 108 are filled therewith. This step is shown in FIG. 3D. Suitable deposition processes include, by way of example and not limitation, plating, solder, atomized nano-particle deposition, CVD, PECVD, sputtering, and the like. The electrically conductive material 112 may comprise a metal including, without limitation, solder, aluminum, titanium, nickel, iridium, copper, gold, tungsten, silver, platinum, palladium, tantalum, ~~molybendum,~~ molybdenum, or alloys of these metals. Alternatively, the electrically conductive material 112 may comprise a conductive polymer, such as a metal-filled silicone, or an isotropically conductive or conductor-filled epoxy. Suitable conductive polymers are sold, for instance, by Epoxy Technology of Billerica, MA. One example is its conductive polymer designated E3114-5. Further suitable conductive polymers include, without limitation, those sold by A.I. Technology of Trenton, N.J.; Sheldahl of Northfield, Minnesota; and 3M of St. Paul, Minnesota. A conductive polymer may be deposited in the trace depressions 108 as a viscous material and subsequently cured as required and may be applied by a dispensing nozzle or squeegee, by spin-coating, or otherwise as known to those of ordinary skill in the art. In a further embodiment, the electrically conductive material 112 may comprise conductive nano-particles.

Please replace paragraph number **[0053]** with the following rewritten paragraph:

[0053] Referring now to FIG. 4B, a desired pattern of one or more trace precursors in the form of trace depressions 108′ may be formed in a surface 113 of the interlevel dielectric layer 114 using a focused laser beam 110′. A representative laser fluence for forming the trace depressions 108′ through an interlevel dielectric layer 114 is from about 2 to about 10 watts/~~per~~ opening at a pulse duration of 20-25 NS, and at a repetition rate of up to several thousand per second. The wavelength of the focused laser beam 110′ may be a standard UV wavelength (*e.g.*, 355 nm) or infrared or green wavelength (*e.g.*, 1064 nm-532 nm). By way of example, the width of the trace depressions 108′ can be from about 10 μm to about 2 mils or greater.

Please replace paragraph number **[0054]** with the following rewritten paragraph:

[0054] Similar to the embodiment in which trace depressions 108 are ablated into a semiconductor substrate 104, the laser machining process of the present invention results in the formation of trace depressions 108′ which taper inward as the depth of the interlevel dielectric layer 114 increases. The trace depressions 108′ may extend through the full thickness of the interlevel dielectric layer 114 such that the semiconductor substrate 104′, including any active areas 116 thereon, may be contacted through the trace depressions 108′, as shown in broken lines in FIG. 4B. Alternatively, and as shown in solid lines in FIGs. 4B-4E, the trace depressions 108′ may extend into the interlevel dielectric layer 114 a distance less than the thickness of the interlevel dielectric layer 114. Each trace depression 108′ may extend the same distance into the interlevel dielectric layer 114 or the trace depressions 108′ may extend into the interlevel dielectric layer 114 by varying distances as shown. As a further option, the trace depressions 108′ may be extended into and even through the semiconductor substrate 104′ (embodiment not shown).

Please replace paragraph number **[0057]** with the following rewritten paragraph:

[0057] Next, as shown in FIG. ~~3E,~~ 4E, the electrically conductive material 112′ may be planarized using, *e.g.*, a mechanical abrasion technique, such as chemical mechanical planarization (CMP), to laterally isolate the electrically conductive material 112′ in the trace depressions 108′.

Please replace paragraph number **[0063]** with the following rewritten paragraph:

[0063] Referring initially to FIG. 5A, a cross-sectional view of an intermediate structure 118 in the fabrication of a semiconductor device structure 120 having a plurality of traces 122 formed in a surface 123 of the semiconductor substrate 124 thereof is shown. As shown in FIG. 5B, a desired pattern of elongated conductive element precursors in the form of one or more trace depressions 126 and one or more discrete conductive structure precursors, *e.g.*, vias 128, may be formed in the surface 123 of the semiconductor substrate 124 using a

focused laser beam 130. The trace depressions 126 and vias 128 may be of any size, shape and depth suitable to define the desired conductive pathway. The vias 128 may extend through the full thickness of the semiconductor substrate 124 (embodiment not shown), or may extend into the semiconductor substrate 124 a depth less than the full thickness thereof as shown.

Please replace paragraph number **[0067]** with the following rewritten paragraph:

[0067] A similar process sequence to that shown in FIGs. 5A-5E may be utilized to ablate one or more elongated conductive elements and one or more discrete conductive structures substantially simultaneously in a semiconductor film such as an interlevel dielectric layer 134. Referring to FIGs. 6A-6E, steps in an exemplary method according to the present invention for fabricating a semiconductor device structure ~~120~~ 120′ having a trace 122′ in combination with a via 128′ in the interlevel dielectric layer 134 thereof are illustrated. It will be understood and appreciated by those of ordinary skill in the art that while in the illustrated process the trace 122′ and via 128′ are formed in an interlevel dielectric layer 134, a similar process may also be utilized to form elongated conductive elements in other films, such as a passivation film (*e.g.*, a silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or parylene film).

Please replace paragraph number **[0068]** with the following rewritten paragraph:

[0068] Referring initially to FIG. 6A, a cross-sectional view of an intermediate structure 118′ in the fabrication of a semiconductor device structure 120′ having a plurality of traces 122′ and one or more vias 128′ formed in a surface 135 of the interlevel dielectric layer 134 thereof is shown. The intermediate structure 118′ includes a semiconductor substrate 124′, *e.g.*, a silicon wafer, having an interlevel dielectric layer 134 (*e.g.*, a SiO_2 layer) thereon. As with the example illustrated in FIGs. 4A-4E, the interlevel dielectric layer 134 may be deposited on the semiconductor substrate 124′ using, for example, CVD techniques.

Please replace paragraph number **[0069]** with the following rewritten paragraph:

[0069] Subsequently, as shown in FIG. 6B, a desired pattern of elongated conductive element precursors in the form of one or more trace depressions 126′ and one or more discrete conductive structure precursors, *e.g.*, vias 128′, may be formed in the surface 135 of the interlevel dielectric layer 134 using a focused laser beam 130′. The trace depressions 126′ and vias 128′ may be of any size, shape and depth suitable to define the desired conductive pathway. The vias 128′ may extend through the full thickness of the interlevel dielectric layer 134, as shown in broken lines in FIG. 6B, such that the semiconductor substrate 124′, including any active areas 136 thereon, may be contacted through the vias 128′. Alternatively, and as shown in solid lines in FIGs. 6B-6E, the vias 128′ may extend into the interlevel dielectric layer 134 a depth less than the thickness of the interlevel dielectric layer 134. As a further option, the vias 128′ may be extended into and even through the semiconductor substrate 124′ (embodiment not shown).